

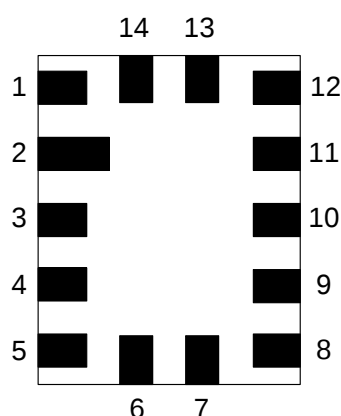
General Description

LSS10020T is a small 14pin QFN packaged customized ASIC with configurable parameters. It support IO expander together with LED dimming.

Features

- Ultra low power consumption.
- Pb - Free and RoHS Compliant and Halogen - Free
- STQFN - 14 Package

Pin Configuration



1.6mm x 2.0mm 14 Pin STQFN
Top View

Ordering Information

Part Number	Package Type
LSS10020T	14-pin QFN, 3k units Tape and Reel

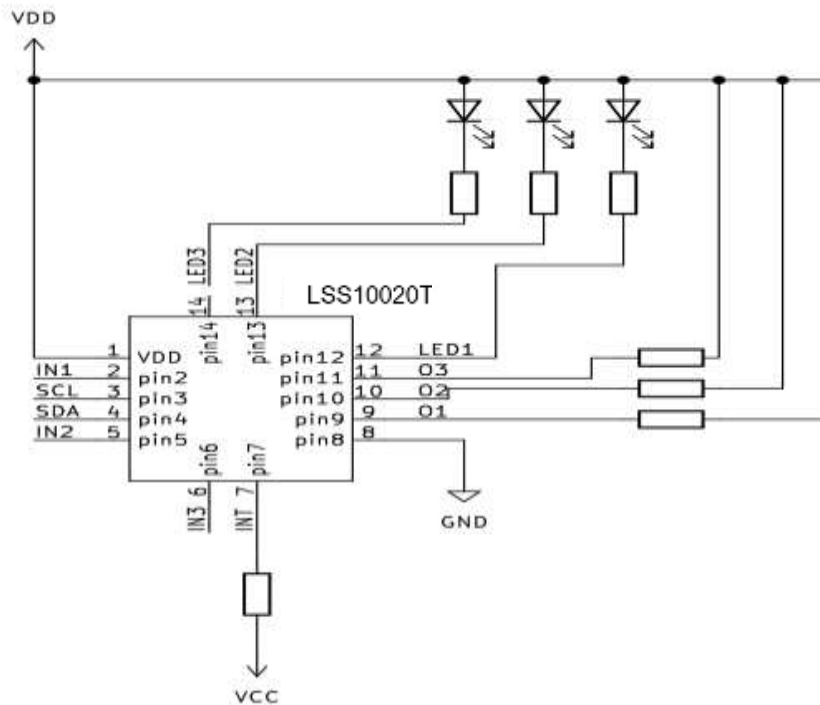
Program Code Version Information

Date	Datasheet Version	Programming Code Version	Lock Status	Checksum	Part Code	Code Version
2022-12-01	.02	002	U	0XB349A669		

Datasheet Revision History

Date	Version	Change
2022-08-11	0.1	Initial version, new design for LS98002 chip
2023-02-23	0.2	Add EN for all led control

Reference Schematic



Note:

1. Voltage on any pin must be within GND to VDD.
2. ESD protection must be considered on all Pins which connected to external interface.

Pin name

Pin	Pin name	TYPE	Function
1	VDD	Power	Power supply.
2	IN1	Digital input	Floating with low voltage input
3	SCL	Digital input	Floating with low voltage input
4	SDA	Digital input/output	Floating with low voltage input/Digital output with open drain
5	IN2	Digital input	Floating with low voltage input
6	IN3	Digital input	Floating with low voltage input
7	INT	Digital output	NMOS open drain with 2x
8	GND	Power GND	Ground of power supply
9	O1	Digital output	NMOS open drain with 2x
10	O2	Digital output	NMOS open drain with 2x
11	O3	Digital output	NMOS open drain with 2x
12	LED1	Digital output	NMOS open drain with 2x
13	LED2	Digital output	NMOS open drain with 2x
14	LED3	Digital output	NMOS open drain with 2x

Customize Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_Q	Quiescent Current	Static inputs and floating outputs	--	0.5	--	μA
F_{led}	LED1/2/3	At temperature 25°C		9.7		KHZ
T_{INT}	Delay 1 Time	At temperature 25°C		20		ms

I2C operation:

I2C Write command: 0x00, I2C Read command: 0x01

一. Read PIN2/PIN5/PIN6 input status

Step 1: Write Register 0x7E, 00; Write Register 0x7D, 00; Both registers' Default value are 0.

Step2: Read Register 0x7C, the bit vs PIN as below:

Bit:

0	VSS
1	PIN2 Digital Input
2	PIN5 Digital Input
3	PIN6 Digital Input
4	PIN7 Digital Input
5	PIN9 Digital Input
6	PIN10 Digital Input
7	PIN11 Digital Input

二: Set PIN9/PIN10/PIN11 output

write Register 0x7B, [data]

[data] BIT vs output

Bit:

0	PIN9	1: Open Drain; 0:Output 0; Default 1
1	PIN10	1: Open Drain; 0:Output 0; Default 1
2	PIN11	1: Open Drain; 0:Output 0; Default 1
3	No use;	Default 0
4	EN_G_12PIN	1: Open Drain; 0:Output 0; Default 0
5	EN_B_13PIN	1: Open Drain; 0:Output 0; Default 0
6	EN_R_14PIN	1: Open Drain; 0:Output 0; Default 0
7	LED Dimming enable ;1. PWM 9.7KHz output; 0: PWM Disable; Default :0	

三: LED1/LED2/LED3 brightness control

Register Address

LED1: 0xCE; LED2: 0xCF; LED3: 0xD0

8bit register value is the PWM duty, from 0 to 100%

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
Supply Voltage on VDD to GND	-0.3	7	V
Maximum Voltage Input to Pins	--	VDD + 0.3	V
VDD to GND Maximum DC Current	--	90	mA
Input Leakage Current	--	1000	nA
Storage Temperature Range	-65	150	°C
Junction Temperature	--	150	°C
ESD Protection (HBM)	2000	--	V
ESD Protection (CDM)	500	--	V
Moisture Sensitivity Level (MSL)	1		

Electrical Characteristics

EC at T = -40°C to +125°C, VDD = 2.3V to 5.5V Unless Otherwise Noted

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage		2.3	5.0	5.5	V
T _A	Operating Temperature		-40	25	85	°C
C _{VDD}	Capacitor Value at VDD		--	0.1	--	μF
V _O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I _{VDD}	Maximum Average or DC Current Through VDD Pin	T _J = 85°C	--	--	90	mA
I _{IH}	HIGH-Level Input Current	Logic Input PINs; V _{IN} = VDD	-1.0	--	1.0	μA
I _{IL}	LOW-Level Input Current	Logic Input PINs; V _{IN} = 0V	-1.0	--	1.0	μA
V _{IH}	HIGH-Level Input Voltage	Logic Input with Schmitt Trigger, at VDD=3.3V				V
		Logic Input with Schmitt Trigger, at VDD=5.0V				V
		Logic Input without Schmitt Trigger, at VDD=3.3V				V
		Logic Input without Schmitt Trigger, at VDD=5.0V				V
		Low Voltage Input, at VDD=3.3V				V

LSS10020T

Enhanced IO expander



		Low Voltage Input, at VDD=5.0V				V
V _{IL}	LOW-Level Input Voltage	Logic Input with Schmitt Trigger, at VDD=3.3V				V
		Logic Input with Schmitt Trigger, at VDD=5.0V				V
		Logic Input without Schmitt Trigger, at VDD=3.3V				V
		Logic Input without Schmitt Trigger, at VDD=5.0V				V
		Low Voltage Input, at VDD=3.3V				V
		Low Voltage Input, at VDD=5.0V				V
V _{OH}	HIGH-Level Output Voltage	Push Pull, 1x Drive I _{OH} = 3mA, at VDD=3.3 V				V
		Push Pull, 1x Drive I _{OH} = 5mA, at VDD=5.0 V				V
		Push Pull, 2x Drive I _{OH} = 3mA, at VDD=3.3 V				V
		Push Pull, 2x Drive I _{OH} = 5mA, at VDD=5.0 V				V
		Open Drain, 1x Drive I _{OH} = 3mA, at VDD=3.3 V				V
		Open Drain, 1x Drive I _{OH} = 3mA, at VDD=5.0 V				V
		Open Drain, 2x Drive I _{OH} = 3mA, at VDD=3.3 V				V
		Open Drain, 2x Drive I _{OH} = 3mA, at VDD=5.0 V				V
V _{OL}	LOW-Level Output Voltage	Push Pull, 1x Drive I _{OH} = 3mA, at VDD=3.3 V				V
		Push Pull, 1x Drive I _{OH} = 5mA, at VDD=5.0 V				V
		Push Pull, 2x Drive I _{OH} = 3mA, at VDD=3.3 V				V
		Push Pull, 2x Drive I _{OH} = 5mA, at VDD=5.0 V				V
		Open Drain, 1x Drive				V

LSS10020T

Enhanced IO expander



		$I_{OH} = 3mA$, at $VDD=3.3 V$				
		Open Drain, 1x Drive $I_{OH} = 3mA$, at $VDD=5.0 V$				V
		Open Drain, 2x Drive $I_{OH} = 3mA$, at $VDD=3.3 V$				V
		Open Drain, 2x Drive $I_{OH} = 3mA$, at $VDD=5.0 V$				V
I_{OH}	HIGH-Level Output Current	Push Pull, $V_{OH} = 2.4 V$, 1X Driver, at $VDD=3.3 V$				mA
		Push Pull, $V_{OH} = 2.4 V$, 1X Driver, at $VDD=5.0 V$				mA
		Push Pull, $V_{OH} = 2.4 V$, 2X Driver, at $VDD=3.3 V$				mA
		Push Pull, $V_{OH} = 2.4 V$, 2X Driver, at $VDD=5.0 V$				mA
		Open Drain, $V_{OH} = 2.4 V$, 1X Driver, at $VDD=3.3 V$				mA
		Open Drain, $V_{OH} = 2.4 V$, 1X Driver, at $VDD=5.0 V$				mA
		Open Drain, $V_{OH} = 2.4 V$, 2X Driver, at $VDD=3.3 V$				mA
		Open Drain, $V_{OH} = 2.4 V$, 2X Driver, at $VDD=5.0 V$				mA
I_{OL}	LOW-Level Output Current	Push Pull, $V_{OH} = 2.4 V$, 1X Driver, at $VDD=3.3 V$				mA
		Push Pull, $V_{OH} = 2.4 V$, 1X Driver, at $VDD=5.0 V$				mA
		Push Pull, $V_{OH} = 2.4 V$, 2X Driver, at $VDD=3.3 V$				mA
		Push Pull, $V_{OH} = 2.4 V$, 2X Driver, at $VDD=5.0 V$				mA
		Open Drain, $V_{OH} = 2.4 V$, 1X Driver, at $VDD=3.3 V$				mA
		Open Drain, $V_{OH} = 2.4 V$, 1X Driver, at $VDD=5.0 V$				mA
		Open Drain, $V_{OH} = 2.4 V$, 2X Driver, at $VDD=3.3 V$				mA
		Open Drain, $V_{OH} = 2.4 V$, 2X Driver, at $VDD=5.0 V$				mA
R_{PULL}	Pull up or down Resistance	1Mohm Pull up or down				MΩ
		100Kohm Pull up or down				kΩ

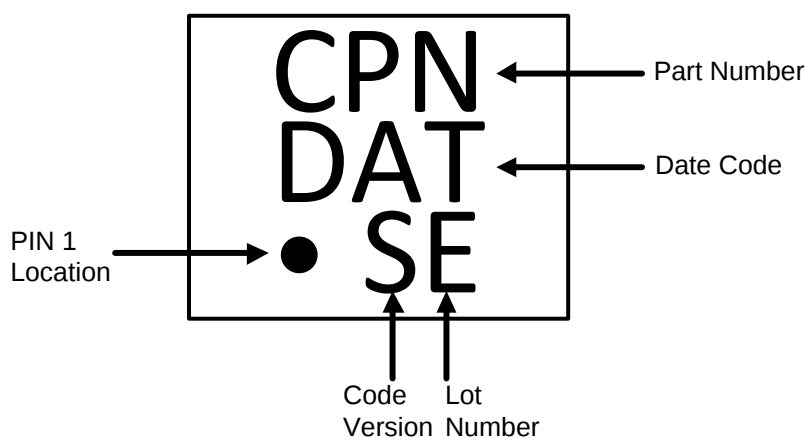
LSS10020T

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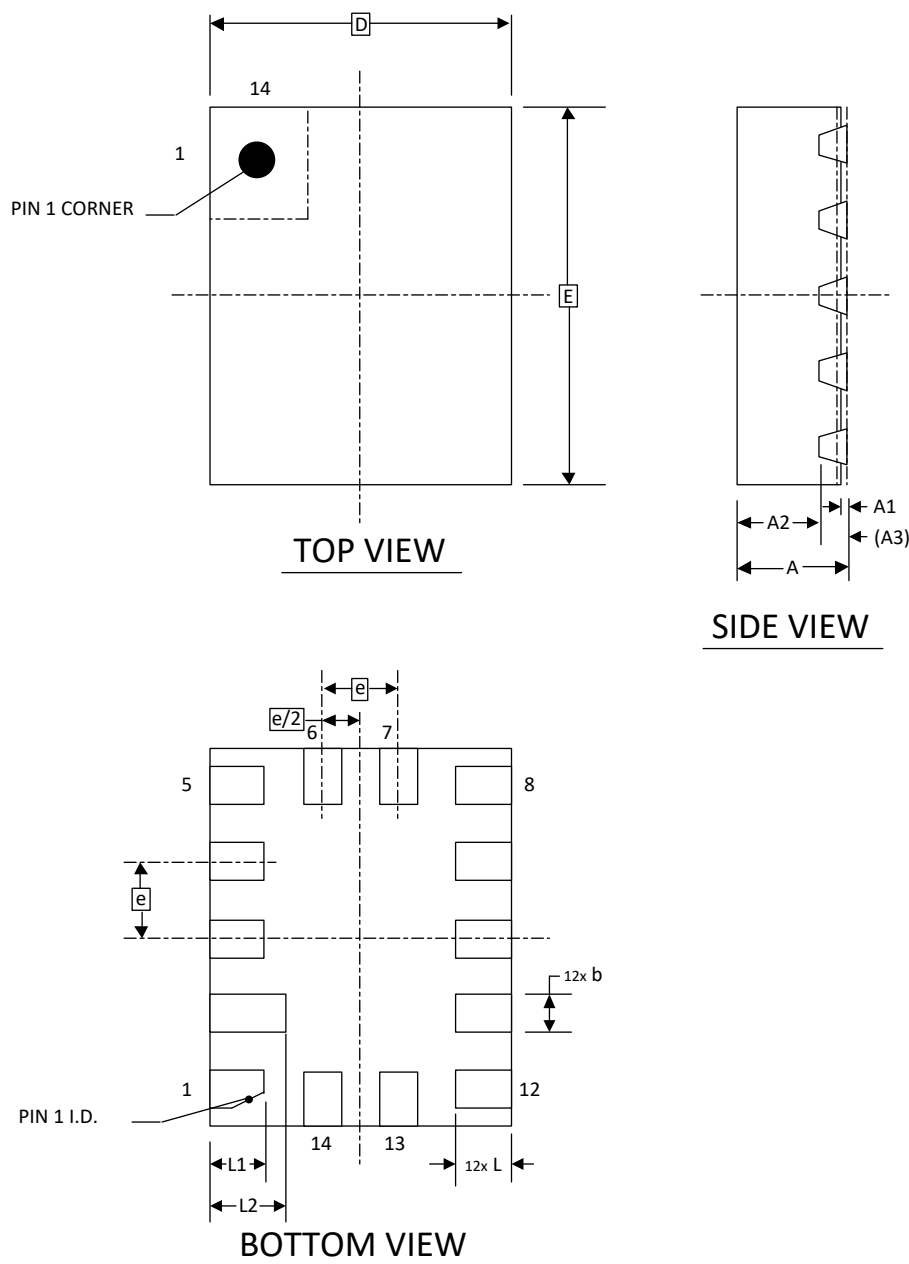


		10Kohm Pull up or down				kΩ
T _{SU}	Startup Time	From VDD rising past PON threshold				ms
PON _{THR}	Power On Threshold	V _{DD} Level Required to Start Up the Chip				V
POFF _{THR}	Power Off Threshold	V _{DD} Level Required to Switch Off the Chip				V
E _{LFOSC}	Error of 2KHz Oscillator	VDD = 2.3V to 5.5V, T = 25°C				%
		VDD = 2.3V to 5.5V, T = -40°C~125°C				%
E _{MFOSC}	Error of 2.5MHz Oscillator	VDD = 2.3V to 5.5V, T = 25°C				%
		VDD = 2.3V to 5.5V, T = -40°C~125°C				%
E _{HFOSC}	Error of 20MHz Oscillator	VDD = 2.3V to 5.5V, T = 25°C				%
		VDD = 2.3V to 5.5V, T = -40°C~125°C				%

Package Top Marking



Package Drawing and Dimensions



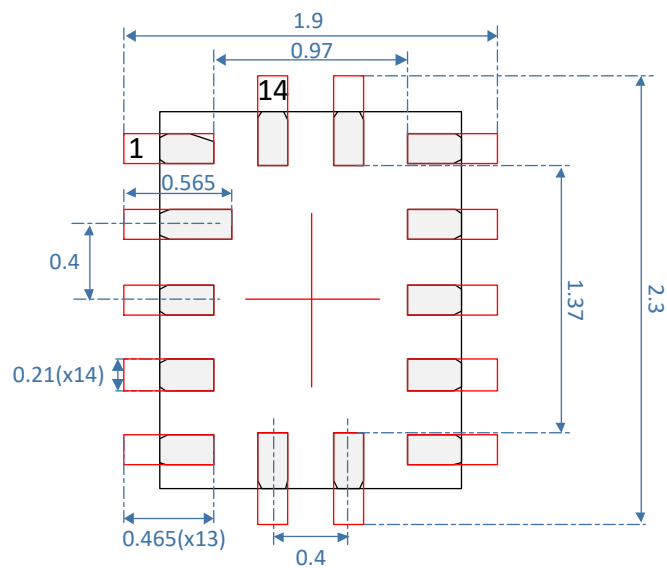
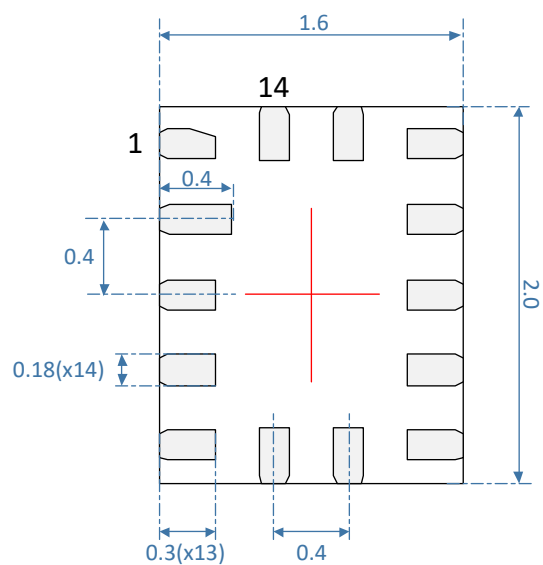
Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.55	1.60	1.65
A1	0.00	0.02	0.05	E	1.95	2.00	2.05
A2	---	0.40	---	L	0.25	0.30	0.35
A3	0.152 REF			L1	0.20	0.30	0.40
b	0.13	0.18	0.23	L2	0.35	0.40	0.45
e	0.40 BSC						

LSS10020T

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Recommended Land Pattern



Unit: mm

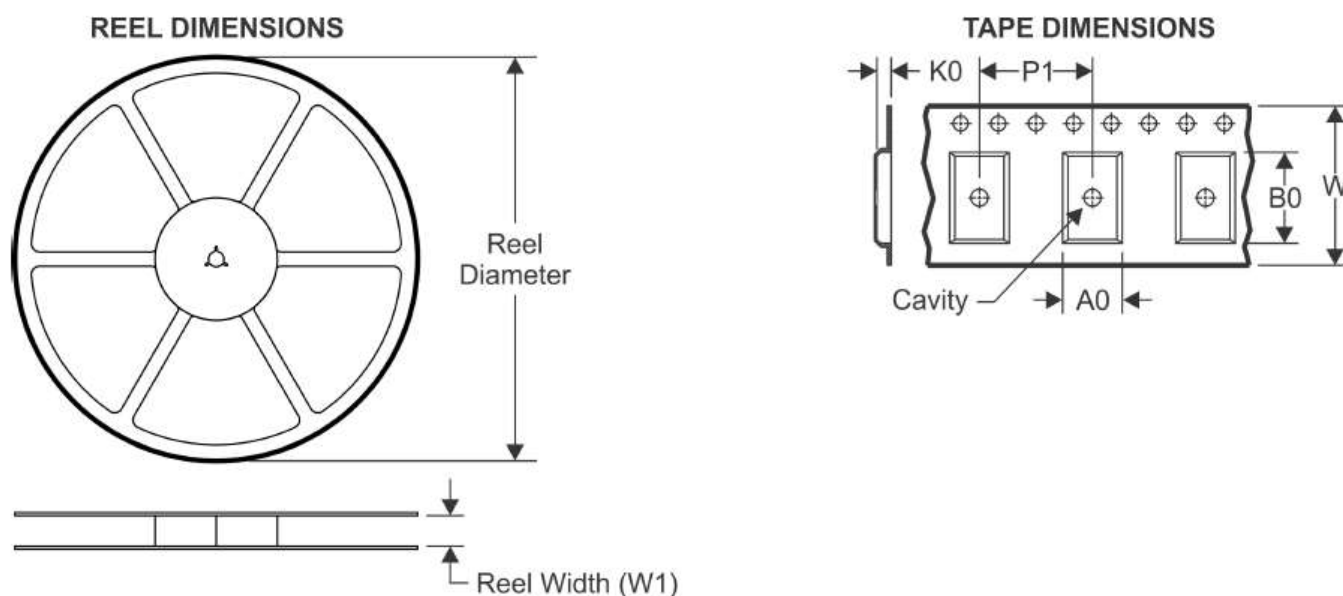
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Tape and Reel Information

Package Type	Num of Pins	Package Size [mm]	Units/package		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			SPQ	1 Box		Pockets	Length [mm]	Pockets	Length [mm]		
QFN 14L 1.6x2.0 mm	14	1.6x2.0x0.55	3000	3000	178/54	30	120	140	560	8	4

Carrier Tape Drawing and Dimensions



A0	Dimension designed to accommodate the component width	1.70mm
B0	Dimension designed to accommodate the component length	2.45mm
K0	Dimension designed to accommodate the component thickness	0.80mm
W	Overall width of the carrier tape	8.00mm
W1	Reel Width	8.40mm
P0	Pitch between Index Hole Pitch	4.00mm
P1	Pitch between successive cavity centers	4.00mm

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020