LSS10025T
Timing control and protections

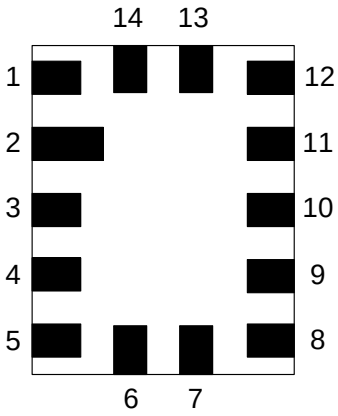
General Description

LSS10025T is a small 14pin QFN packaged customized ASIC with configurable parameters. It support Timing control, UV/OV/OCP functions .

Features

• Ultra-low power consumption.
• Pb - Free and RoHS Compliant and Halogen - Free
• STQFN - 14 Package

Pin Configuration



1.6mm x 2.0mm 14 Pin STQFN
Top View

Ordering Information

Part Number	Package Type
LSS10025T	14-pin QFN, 3k units Tape and Reel

Program Code Version Information

Date	Datasheet Version	Programming Code Version	Lock Status	Checksum	Part Code	Code Version
2023-12-21	.01	001	L	0xF5690FA2	C27	A

Datasheet Revision History

Date	Version	Change
2023-12-21	0.1	Initial version, new design for LS98102 chip

Reference Schematic

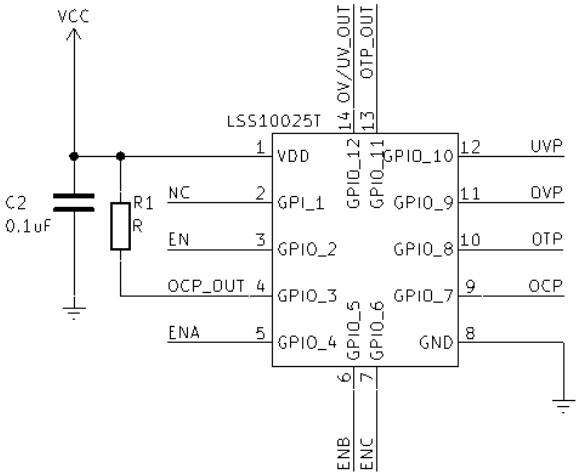


Figure 1. Typical application diagram

Note:

1. Voltage on any pin must be with in GND to VDD.
2. ESD protect is must be considered on all Pins which connected to external interface.

Pin name

Pin	Pin name	TYPE	Function
1	VDD	Power	Power supply.2.3V-5.5V, power supply voltage shall not be less than 2.5V
2	NC	NC	NC
3	EN	Logic Input with Schmitt Trigger	Power up and down control signal
4	OCP_OUT	1× open-drain digital output	Overcurrent detection, digital output signal
5	ENA	1× push-pull Digital output	Delay signal A
6	ENB	1× push-pull Digital output	Delay signal B
7	ENC	1× push-pull Digital output	Delay signal C
8	GND	Power	Ground of power supply
9	OCP_DET	Analog signal IO input	Overcurrent detection input
10	OTP_DET	Analog signal IO input	Over temperature detection input
11	OVP_DET	Analog signal IO input	Overvoltage detection input
12	UVP_DET	Analog signal IO input	Undervoltage detection input
13	OTP_OUT	2× open-drain digital output	Over temperature detection output
14	OV/UV_OUT	2× open-drain digital output	Overvoltage and undervoltage detection output

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
Supply Voltage on VDD to GND	-0.3	7	V
Maximum Voltage Input to Pins	-0.3	7	V
VDD to GND Maximum DC Current	--	90	mA
Input Leakage Current	--	1000	nA
Storage Temperature Range	-65	150	℃
Junction Temperature	--	150	℃
ESD Protection (HBM)	2000	--	V
ESD Protection (CDM)	500	--	V
Moisture Sensitivity Level (MSL)	1		

Customize Electrical Characteristics

VDD =3.3V±10%, Temp=25℃

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_Q	Quiescent Current	Static inputs and floating outputs	--	30	--	μA
T_{DLY}	Power up and down delay output time	At temperature 25℃	--	10	--	ms
V_{OCP}	Protection threshold	25℃@VDD=3.3V	--	2.5	--	V
	Recovery threshold	25℃@VDD=3.3V	--	1.25	--	V
V_{OTP}	Protection threshold	25℃@VDD=3.3V	--	2.5	--	V
	Recovery threshold	25℃@VDD=3.3V	--	1.25	--	V
V_{OVP}	Protection threshold	25℃@VDD=3.3V	--	1.25	--	V
	Recovery threshold	25℃@VDD=3.3V	--	1.2	--	V
V_{UVP}	Protection threshold	25℃@VDD=3.3V	--	1.25	--	V
	Recovery threshold	25℃@VDD=3.3V	--	1.2	--	V

Electrical Characteristics

EC at T = -40℃ to +85℃, VDD = 2.3V to 5.5V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		2.3	3.3	5.5	V
T_A	Operating Temperature		-40	25	85	℃
C_{VDD}	Capacitor Value at VDD		--	0.1	--	μF
I_{IH}	HIGH-Level Input Current	Logic Input PINs; V_{IN} = VDD	-1.0	--	1.0	μA
I_{IL}	LOW-Level Input Current	Logic Input PINs; V_{IN} = 0V	-1.0	--	1.0	μA

IO PIN						
V_{IH}	HIGH-Level Input Voltage	Logic Input with Schmitt Trigger, at VDD=2.5V	0.8*VDD	--	--	V
		Logic Input with Schmitt Trigger, at VDD=3.3V	0.8*VDD	--	--	V
		Logic Input with Schmitt Trigger, at VDD=5.0V	0.8*VDD	--	--	V
		Logic Input without Schmitt Trigger, at VDD=2.5V	0.7*VDD	--	--	V
		Logic Input without Schmitt Trigger, at VDD=3.3V	0.7*VDD	--	--	V
		Logic Input without Schmitt Trigger, at VDD=5.0V	0.7*VDD	--	--	V
		Low Voltage Input, at VDD=2.5V	0.82	--	--	V
		Low Voltage Input, at VDD=3.3V	0.92	--	--	V
		Low Voltage Input, at VDD=5.0V	1.00	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input with Schmitt Trigger, at VDD=2.5V	--	--	0.2*VDD	V
		Logic Input with Schmitt Trigger, at VDD=3.3V	--	--	0.2*VDD	V
		Logic Input with Schmitt Trigger, at VDD=5.0V	--	--	0.2*VDD	V
		Logic Input without Schmitt Trigger, at VDD=2.5V	--	--	0.3*VDD	V
		Logic Input without Schmitt Trigger, at VDD=3.3V	--	--	0.3*VDD	V
		Logic Input without Schmitt Trigger, at VDD=5.0V	--	--	0.3*VDD	V

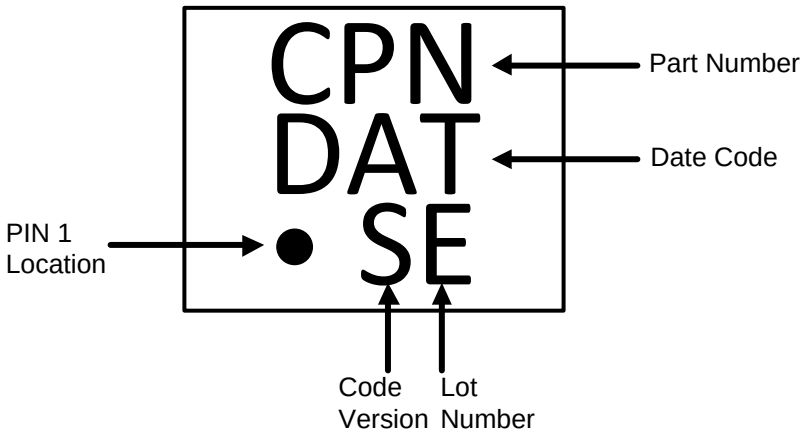
		Low Voltage Input, at VDD=2.5V	--	--	0.68	V
		Low Voltage Input, at VDD=3.3V	--	--	0.75	V
		Low Voltage Input, at VDD=5.0V	--	--	0.85	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger, at VDD=2.5V	--	0.42	--	V
		Logic Input with Schmitt Trigger, at VDD=3.3V	--	0.45	--	V
		Logic Input with Schmitt Trigger, at VDD=5V	--	0.54	--	V
I_{LKG}	Input leakage (Absolute Value)		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage	Push Pull, 1x Drive I_{OH} = 1mA, at VDD=2.5 V	2.02	--	--	V
		Push Pull, 1x Drive I_{OH} = 3mA, at VDD=3.3 V	2.60	--	--	V
		Push Pull,1x Drive I_{OH} = 5mA, at VDD=5.0 V	4.04	--	--	V
		Push Pull, 2x Drive I_{OH} = 1mA, at VDD=2.5 V	2.10	--	--	V
		Push Pull, 2x Drive I_{OH} = 3mA, at VDD=3.3 V	2.80	--	--	V
		Push Pull, 2x Drive I_{OH} = 5mA, at VDD=5.0 V	4.20	--	--	V
V_{OL}	LOW-Level Output Voltage	Push Pull, 1x Drive I_{OL} = 1mA, at VDD=2.5 V	--	--	0.11	V
		Push Pull, 1x Drive I_{OL} = 3mA, at VDD=3.3 V	--	--	0.25	V
		Push Pull,1x Drive I_{OL} = 5mA, at VDD=5.0 V	--	--	0.29	V
		Push Pull, 2x Drive I_{OL} = 1mA, at VDD=2.5 V	--	--	0.06	V
		Push Pull, 2x Drive I_{OL} = 3mA, at VDD=3.3 V	--	--	0.22	V
		Push Pull, 2x Drive I_{OL} = 5mA, at VDD=5.0 V	--	--	0.21	V
		Open Drain, 1x Drive I_{OL} = 1mA, at VDD=2.5 V	--	--	0.077	V

		Open Drain, 1x Drive I_{OL} = 3mA, at VDD=3.3 V	--	--	0.12	V
		Open Drain, 1x Drive I_{OL} = 3mA, at VDD=5.0 V	--	--	0.15	V
		Open Drain, 2x Drive I_{OL} = 1mA, at VDD=2.5 V	--	--	0.075	V
		Open Drain, 2x Drive I_{OL} = 3mA, at VDD=3.3 V	--	--	0.089	V
		Open Drain, 2x Drive I_{OL} = 3mA, at VDD=5.0 V	--	--	0.114	V
I_{OH}	HIGH-Level Output Pulse Current (see Note)	Push Pull, V_{OH} = VDD-0.2 V, 1X Driver, at VDD=2.5 V	1.37	--	--	mA
		Push Pull, V_{OH} = 2.4 V, 1X Driver, at VDD=3.3 V	5	--	--	mA
		Push Pull, V_{OH} = 2.4 V, 1X Driver, at VDD=5.0 V	19	--	--	mA
		Push Pull, V_{OH} = VDD-0.2 V, 2X Driver, at VDD=2.5 V	2.74	--	--	mA
		Push Pull, V_{OH} = 2.4 V, 2X Driver, at VDD=3.3 V	10	--	--	mA
		Push Pull, V_{OH} = 2.4 V, 2X Driver, at VDD=5.0 V	38	--	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note)	Push Pull, V_{OL} = 0.15 V, 1X Driver, at VDD=2.5 V	1.61	--	--	mA
		Push Pull, V_{OL} = 0.4 V, 1X Driver, at VDD=3.3 V	5	--	--	mA
		Push Pull, V_{OL} = 0.4 V, 1X Driver, at VDD=5.0 V	7	--	--	mA
		Push Pull, V_{OL} = 0.15 V, 2X Driver, at VDD=2.5 V	3.22	--	--	mA
		Push Pull, V_{OL} = 0.4 V, 2X Driver, at VDD=3.3 V	10	--	--	mA
		Push Pull, V_{OL} = 0.4 V, 2X Driver, at VDD=5.0 V	14	--	--	mA
		Open Drain, V_{OL} = 0.15 V, 1X Driver, at VDD=2.5 V	4.9	--	--	mA
		Open Drain, V_{OL} = 0.4 V, 1X Driver, at VDD=3.3 V	15	--	--	mA
		Open Drain, V_{OL} = 0.4 V, 1X Driver, at VDD=5.0 V	21	--	--	mA

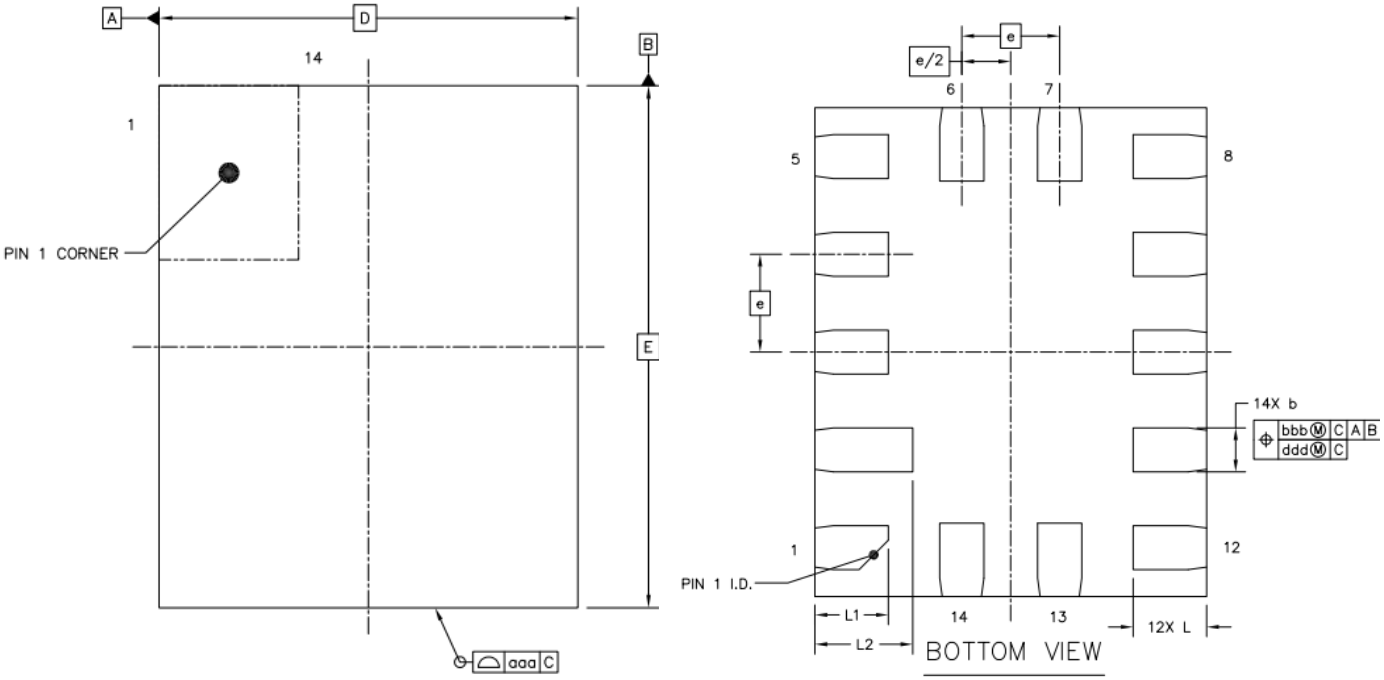
		Open Drain, V_{OL} = 0.15 V, 2X Driver, at VDD=2.5 V	9.8	--	--	mA
		Open Drain, V_{OL} = 0.4 V, 2X Driver, at VDD=3.3 V	30	--	--	mA
		Open Drain, V_{OL} = 0.4 V, 2X Driver, at VDD=5.0 V	42	--	--	mA
ACMPH Specifications						
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	VDD	V
		Negative Input	0	--	1.23	V
V_{offset}	ACMP Input Offset		-5	2	5	mV
Input Buffer	Bandwidth		--	500	--	KHz
	Offset		-9.6	4.8	9.6	mV
	Power Consumption		--	2	--	
t_{start}	ACMP Startup Time when BG ON	ACMP Power-On delay, Minimal required wake time for the "Wake and Sleep function", for ACMPxH	--	29	--	uS
	ACMP Startup Time when BG Off		--	1	--	mS
R_{sin}	Series Input Resistance	Gain = 1/2	1.2	1.34	1.48	MΩ
		Gain = 1/5	1.2	1.34	1.48	MΩ
PROP	Propagation Delay, Response Time	Overdrive = 50 mV	--	0.318	0.402	uS
G	Gain	G=1/2	0.4943	0.5	0.5057	
		G=1/5	0.1980	0.2	0.2019	
Vref	Internal Vref error, Vref=0 to1.23V	T=25°C	--	5	--	mV
		T=-40°C to+85°C	-1.5%	--	1.5%	Fs
Power Consumption		Internal Vref Without Input Buffer	--	10	--	uA
ACMPL Specifications						
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	VDD	V
		Negative Input	0	--	1.23	V
V_{offset}	ACMP Input Offset	--	-5	2	5	mV
t_{start}	ACMP Startup Time when BG ON	ACMP Power-On delay, Minimal required wake time for the "Wake and Sleep function", for ACMPxL	--	108	--	uS
	ACMP Startup Time when BG Off		--	1	--	mS
R_{sin}	Series Input Resistance	Gain = 1/2 (ACMP- = 0.6V)	1.2	1.34	1.48	MΩ
		Gain = 1/5 (ACMP- = 1.1V)	1.2	1.34	1.48	MΩ

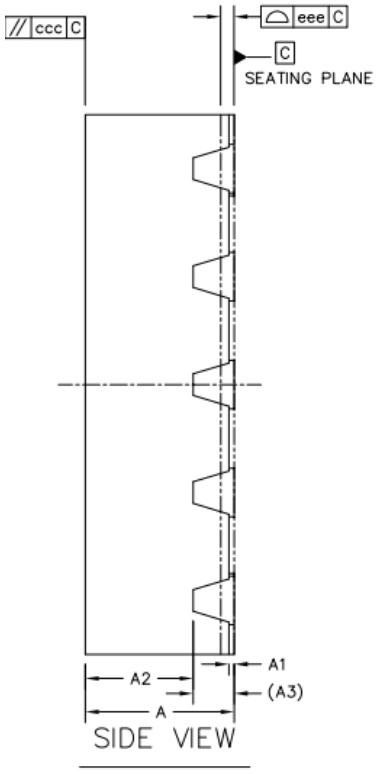
PROP	Propagation Delay, Response Time	Overdrive = 50 mV	--	6.477	8.159	uS
G	Gain	G=1/2 (ACMP- = 0.6V)	0.4968	0.5	0.5032	
		G=1/5 (ACMP- = 1.1V)	0.1975	0.2	0.2025	
Vref	Internal Vref error, Vref=0 to1.23V	T=25°C	--	5	--	mV
		T=-40°C to +85°C	-1.5%	--	1.5%	Fs
Power Consumption		Internal Vref	--	4.2	--	uA
Note: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.						

Package Top Marking



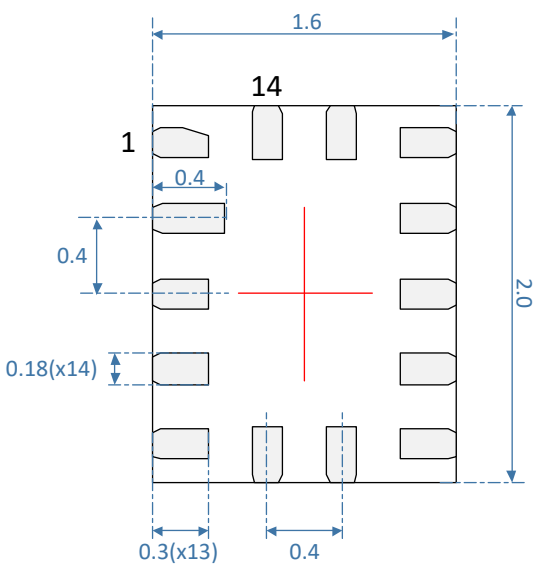
Package Drawing and Dimensions

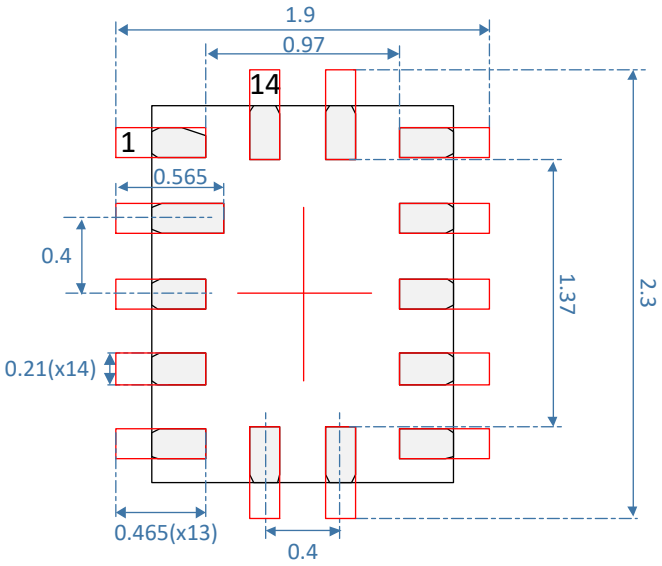




		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.4	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.13	0.18	0.23
BODY SIZE	X	D		1.6 BSC	
	Y	E		2 BSC	
LEAD PITCH		e		0.4 BSC	
LEAD LENGTH		L	0.25	0.3	0.35
		L1	0.2	0.3	0.4
		L2	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.05	
LEAD OFFSET		bbb		0.07	
		ddd		0.05	

Recommended Land Pattern



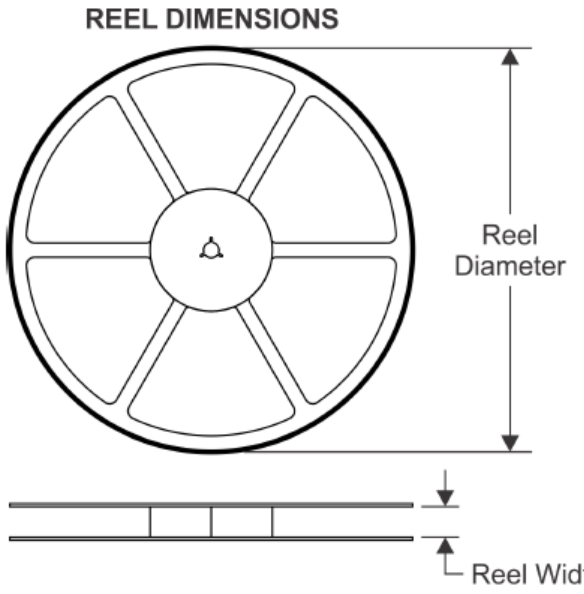


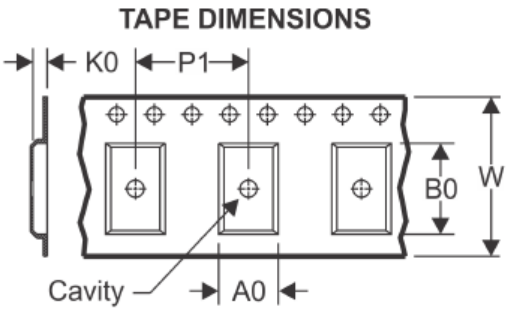
Unit: mm

Tape and Reel Information

Package Type	Num of Pins	Package Size [mm]	Units/package		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			SPQ	1 Box		Pockets	Length [mm]	Pockets	Length [mm]		
QFN 14L 1.6x2.0 mm	14	1.6x2.0x0.55	3000	3000	178/54	30	120	140	560	8	4

Carrier Tape Drawing and Dimensions





A0	Dimension designed to accommodate the component width	1.76mm
B0	Dimension designed to accommodate the component length	2.16mm
K0	Dimension designed to accommodate the component thickness	0.73mm
W	Overall width of the carrier tape	8.00mm
W1	Reel Width	9.50mm
P0	Pitch between Index Hole Pitch	4.00mm
P1	Pitch between successive cavity centers	4.00mm

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020