LSS10031T
Voltage Detect, Watchdog and level shift

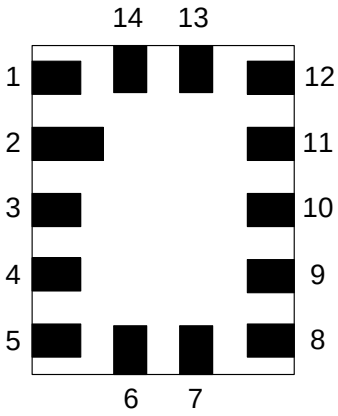
General Description

LSS10031T is a small 14pin QFN packaged customized ASIC with configurable parameters. It support Voltage Detect ,Watchdog and level shift

Features

- Ultra-low power consumption.
- Pb - Free and RoHS Compliant and Halogen - Free
- STQFN - 14 Package

Pin Configuration



1.6mm x 2.0mm 14 Pin STQFN
Top View

Ordering Information

Part Number	Package Type
LSS10031T	14-pin QFN, 3k units Tape and Reel

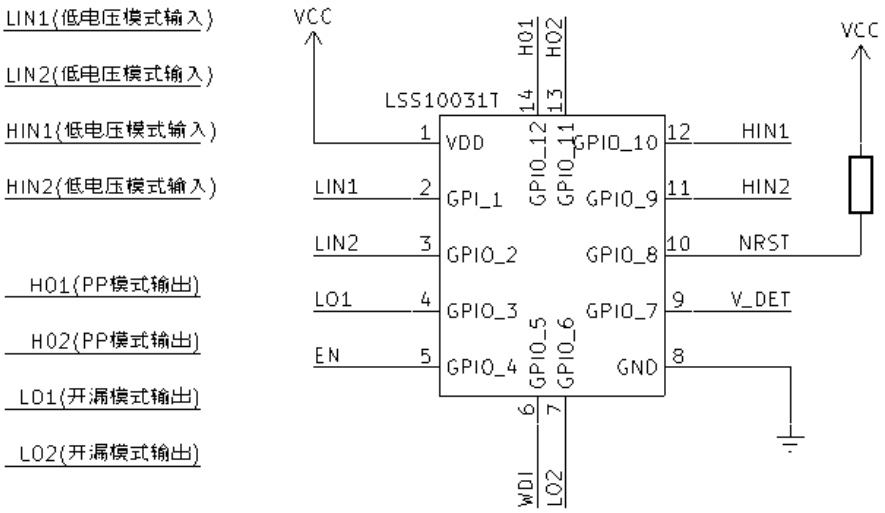
Program Code Version Information

Date	Datasheet Version	Programming Code Version	Lock Status	Checksum	Part Code	Code Version
2023-12-14	0.1	001	L	0X95820DF	C25	A

Datasheet Revision History

Date	Version	Change
2023-12-14	0.1	Initial version, new design for LS98102 chip

Reference Schematic



Note:

1. Voltage on any pin must be with in GND to VDD.
2. ESD protect is must be considered on all Pins which connected to external interface.

Pin name

Pin	Pin name	TYPE	Function
1	VDD	Power	Power supply input，2.3V~5.5V，supply voltage can not be lower than 2.9V
2	Lin1	Low Voltage Input	1.8V port I/O input 1
3	Lin2	Low Voltage Input	1.8V port I/O input 2
4	LO1	Low Voltage Open Drain Output	1.8V port I/O output 1
5	EN	Without Schmidt trigger, digital input	The watchdog enables the input signal
6	WDI	Without Schmidt trigger, digital input	The watchdog feeds the dog input signal
7	LO2	Low Voltage Open Drain Output	1.8V port IO output 2
8	GND	Power Ground	Ground
9	V_DET	Analog voltage input	Voltage sensing input
10	NRST	1x Open Drain Output	NRST output for watch dog and voltage detector
11	HIN2	High voltage digital input	High voltage digital input for HIN2
12	HIN1	High voltage digital input	High voltage digital input for HIN1
13	HO2	2x Push Pull Digital Output	High voltage output for level shift
14	HO1	2x Push Pull Digital Output	High voltage output for level shift

Customize Electrical Characteristics

VDD =3.3V±10%, Temp=25°C

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_Q	Quiescent Current	Static inputs and floating outputs	--	8	--	μA
T_{WD}	Watchdog Time	At temperature 25℃		80		s
T_{nRST}	Low Reset Time	At temperature 25℃		200		ms
V_{DET}	Voltage Detect of ACMP	At VDD = 3.3V		2.9		V

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
Supply Voltage on VDD to GND	-0.3	7	V
Maximum Voltage Input to Pins	--	VDD + 0.3	V
VDD to GND Maximum DC Current	--	90	mA
Input Leakage Current	--	1000	nA
Storage Temperature Range	-65	150	°C
Junction Temperature	--	150	°C
ESD Protection (HBM)	2000	--	V
ESD Protection (CDM)	500	--	V
Moisture Sensitivity Level (MSL)	1		

Electrical Characteristics

EC at T = -40℃ to +85℃, VDD = 2.3V to 5.5V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		2.3	5.0	5.5	V
T_A	Operating Temperature		-40	25	85	°C
C_{VDD}	Capacitor Value at VDD		--	0.1	--	μF
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_{VDD}	Maximum Average or DC Current Through VDD Pin	T_J = 85°C	--	--	90	mA
I_{IH}	HIGH-Level Input Current	Logic Input PINs; V_{IN} = VDD	-1.0	--	1.0	μA
I_{IL}	LOW-Level Input Current	Logic Input PINs; V_{IN} = 0V	-1.0	--	1.0	μA

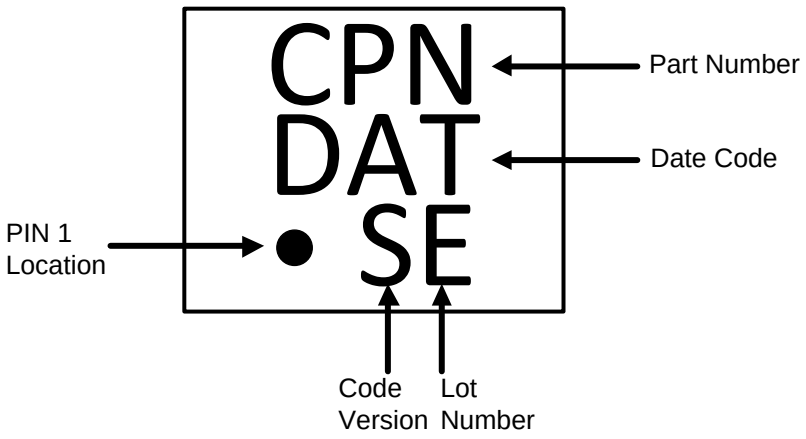
IO PIN						
V_{IH}	HIGH-Level Input Voltage	Logic Input with Schmitt Trigger, at VDD=2.5V	0.8*VDD	--	--	V
		Logic Input with Schmitt Trigger, at VDD=3.3V	0.8*VDD	--	--	V
		Logic Input with Schmitt Trigger, at VDD=5.0V	0.8*VDD	--	--	V
		Logic Input without Schmitt Trigger, at VDD=2.5V	0.7*VDD	--	--	V
		Logic Input without Schmitt Trigger, at VDD=3.3V	0.7*VDD	--	--	V
		Logic Input without Schmitt Trigger, at VDD=5.0V	0.7*VDD	--	--	V
		Low Voltage Input, at VDD=2.5V	0.82	--	--	V
		Low Voltage Input, at VDD=3.3V	0.92	--	--	V
		Low Voltage Input, at VDD=5.0V	1.00	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input with Schmitt Trigger, at VDD=2.5V	--	--	0.2*VDD	V
		Logic Input with Schmitt Trigger, at VDD=3.3V	--	--	0.2*VDD	V
		Logic Input with Schmitt Trigger, at VDD=5.0V	--	--	0.2*VDD	V
		Logic Input without Schmitt Trigger, at VDD=2.5V	--	--	0.3*VDD	V
		Logic Input without Schmitt Trigger, at VDD=3.3V	--	--	0.3*VDD	V
		Logic Input without Schmitt Trigger, at VDD=5.0V	--	--	0.3*VDD	V

		Low Voltage Input, at VDD=2.5V	--	--	0.68	V
		Low Voltage Input, at VDD=3.3V	--	--	0.75	V
		Low Voltage Input, at VDD=5.0V	--	--	0.85	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger, at VDD=2.5V	--	0.42	--	V
		Logic Input with Schmitt Trigger, at VDD=3.3V	--	0.45	--	V
		Logic Input with Schmitt Trigger, at VDD=5V	--	0.54	--	V
I_{LKG}	Input leakage (Absolute Value)		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage	Push Pull, 1x Drive I_{OH} = 1mA, at VDD=2.5 V	2.02	--	--	V
		Push Pull, 1x Drive I_{OH} = 3mA, at VDD=3.3 V	2.60	--	--	V
		Push Pull,1x Drive I_{OH} = 5mA, at VDD=5.0 V	4.04	--	--	V
		Push Pull, 2x Drive I_{OH} = 1mA, at VDD=2.5 V	2.10	--	--	V
		Push Pull, 2x Drive I_{OH} = 3mA, at VDD=3.3 V	2.80	--	--	V
		Push Pull, 2x Drive I_{OH} = 5mA, at VDD=5.0 V	4.20	--	--	V
V_{OL}	LOW-Level Output Voltage	Push Pull, 1x Drive I_{OL} = 1mA, at VDD=2.5 V	--	--	0.11	V
		Push Pull, 1x Drive I_{OL} = 3mA, at VDD=3.3 V	--	--	0.25	V
		Push Pull,1x Drive I_{OL} = 5mA, at VDD=5.0 V	--	--	0.29	V
		Push Pull, 2x Drive I_{OL} = 1mA, at VDD=2.5 V	--	--	0.06	V
		Push Pull, 2x Drive I_{OL} = 3mA, at VDD=3.3 V	--	--	0.22	V
		Push Pull, 2x Drive I_{OL} = 5mA, at VDD=5.0 V	--	--	0.21	V
		Open Drain, 1x Drive I_{OL} = 1mA, at VDD=2.5 V	--	--	0.077	V

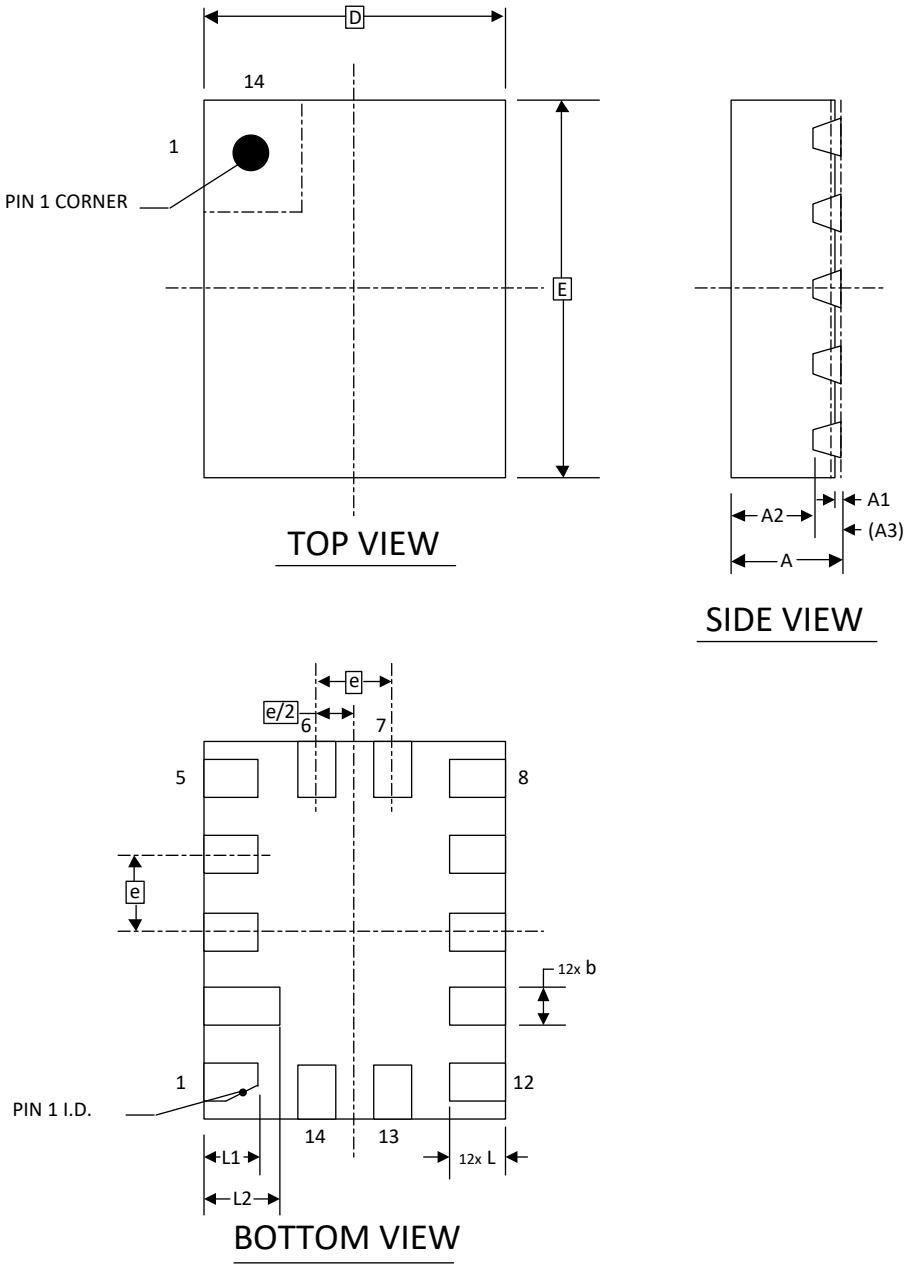
		Open Drain, 1x Drive I_{OL} = 3mA, at VDD=3.3 V	--	--	0.12	V
		Open Drain, 1x Drive I_{OL} = 3mA, at VDD=5.0 V	--	--	0.15	V
		Open Drain, 2x Drive I_{OL} = 1mA, at VDD=2.5 V	--	--	0.075	V
		Open Drain, 2x Drive I_{OL} = 3mA, at VDD=3.3 V	--	--	0.089	V
		Open Drain, 2x Drive I_{OL} = 3mA, at VDD=5.0 V	--	--	0.114	V
I_{OH}	HIGH-Level Output Pulse Current (see Note)	Push Pull, V_{OH} = VDD-0.2 V, 1X Driver, at VDD=2.5 V	1.37	--	--	mA
		Push Pull, V_{OH} = 2.4 V, 1X Driver, at VDD=3.3 V	5	--	--	mA
		Push Pull, V_{OH} = 2.4 V, 1X Driver, at VDD=5.0 V	19	--	--	mA
		Push Pull, V_{OH} = VDD-0.2 V, 2X Driver, at VDD=2.5 V	2.74	--	--	mA
		Push Pull, V_{OH} = 2.4 V, 2X Driver, at VDD=3.3 V	10	--	--	mA
		Push Pull, V_{OH} = 2.4 V, 2X Driver, at VDD=5.0 V	38	--	--	mA
I_{OL}	LOW-Level Output Pulse Current (see Note)	Push Pull, V_{OL} = 0.15 V, 1X Driver, at VDD=2.5 V	1.61	--	--	mA
		Push Pull, V_{OL} = 0.4 V, 1X Driver, at VDD=3.3 V	5	--	--	mA
		Push Pull, V_{OL} = 0.4 V, 1X Driver, at VDD=5.0 V	7	--	--	mA
		Push Pull, V_{OL} = 0.15 V, 2X Driver, at VDD=2.5 V	3.22	--	--	mA
		Push Pull, V_{OL} = 0.4 V, 2X Driver, at VDD=3.3 V	10	--	--	mA
		Push Pull, V_{OL} = 0.4 V, 2X Driver, at VDD=5.0 V	14	--	--	mA
		Open Drain, V_{OL} = 0.15 V, 1X Driver, at VDD=2.5 V	4.9	--	--	mA
		Open Drain, V_{OL} = 0.4 V, 1X Driver, at VDD=3.3 V	15	--	--	mA
		Open Drain, V_{OL} = 0.4 V, 1X Driver, at VDD=5.0 V	21	--	--	mA
		Open Drain, V_{OL} = 0.15 V, 2X Driver, at VDD=2.5 V	9.8	--	--	mA

		Open Drain, V_{OL} = 0.4 V, 2X Driver, at VDD=3.3 V	30	--	--	mA
		Open Drain, V_{OL} = 0.4 V, 2X Driver, at VDD=5.0 V	42	--	--	mA
R_{PULL}	Pull up or down Resistance	1Mohm Pull up or down	--	1	--	MΩ
		100Kohm Pull up or down	--	100	--	kΩ
		10Kohm Pull up or down	--	10	--	kΩ
T_{SU}	Startup Time	From VDD rising past PON threshold	--	1.20	--	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.67	1.80	1.92	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.95	1.25	1.54	V
Note: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.						

Package Top Marking



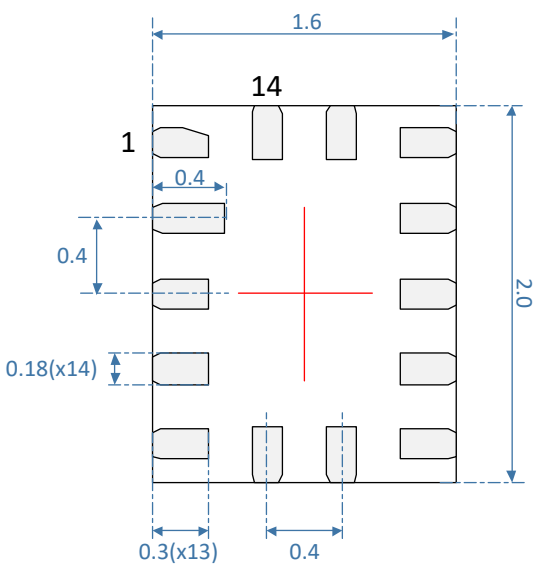
Package Drawing and Dimensions

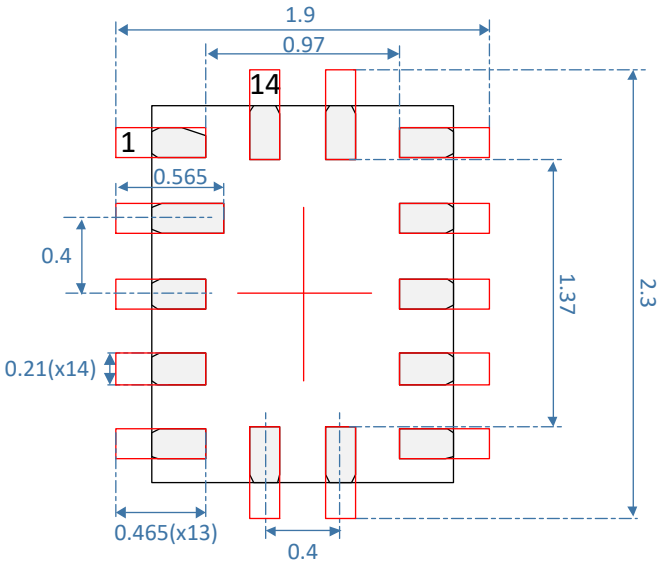


Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.55	1.60	1.65
A1	0.00	0.02	0.05	E	1.95	2.00	2.05
A2	---	0.40	---	L	0.25	0.30	0.35
A3	0.152 REF			L1	0.20	0.30	0.40
b	0.13	0.18	0.23	L2	0.35	0.40	0.45
e	0.40 BSC						

Recommended Land Pattern



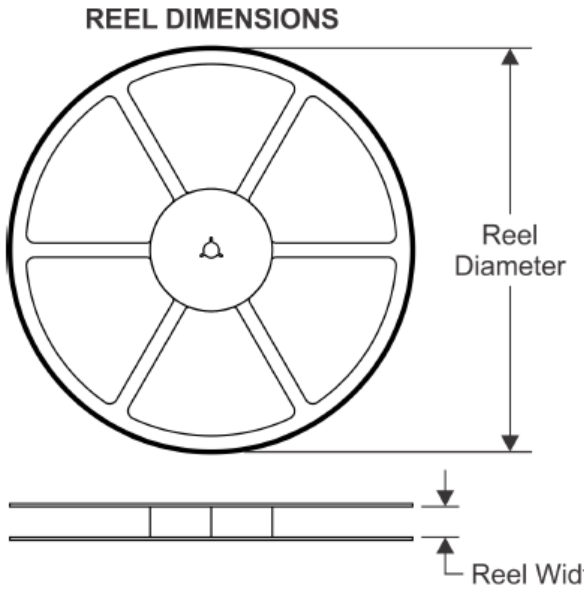


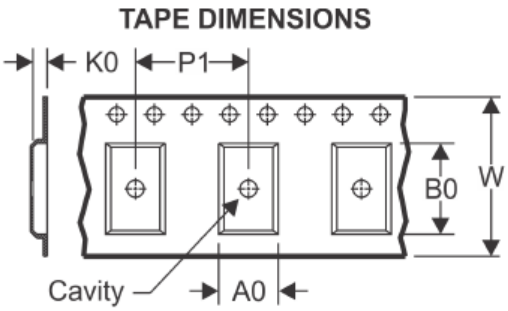
Unit: mm

Tape and Reel Information

Package Type	Num of Pins	Package Size [mm]	Units/package		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			SPQ	1 Box		Pockets	Length [mm]	Pockets	Length [mm]		
QFN 14L 1.6x2.0 mm	14	1.6x2.0x0.55	3000	3000	178/54	30	120	140	560	8	4

Carrier Tape Drawing and Dimensions





A0	Dimension designed to accommodate the component width	1.70mm
B0	Dimension designed to accommodate the component length	2.45mm
K0	Dimension designed to accommodate the component thickness	0.80mm
W	Overall width of the carrier tape	8.00mm
W1	Reel Width	8.40mm
P0	Pitch between Index Hole Pitch	4.00mm
P1	Pitch between successive cavity centers	4.00mm

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020