LSS5010T
Multi-time Watchdog

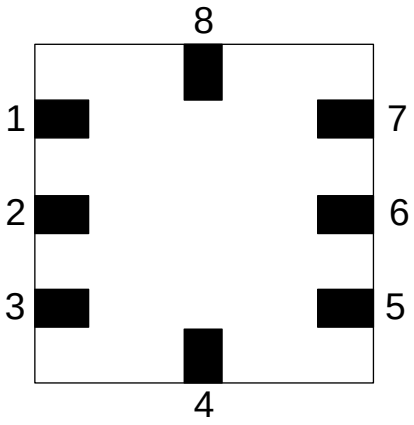
General Description

LSS5010T-A/D is a small 8pin TQFN/DFN packaged customized ASIC with configurable parameters. It supports four selectable watch time.

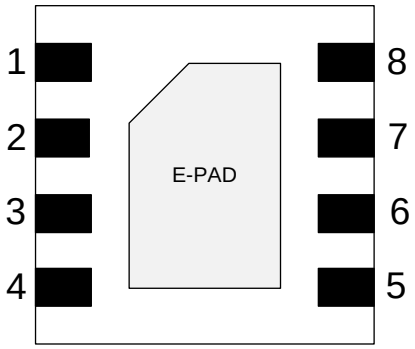
Features

• Ultra-low power consumption.
• Pb - Free and RoHS Compliant and Halogen - Free
• TQFN - 8 Package/DFN- 8 Package

Pin Configuration



LS98003-A
1.3mm x 1.3mm 8 Pin TQFN
Top View



LS98003-D
2.0mm x 2.0mm 8 Pin DFN
Top View

Ordering Information

Part Number	Package Type
LSS5010T	8-pin TQFN/DFN, 3k units Tape and Reel

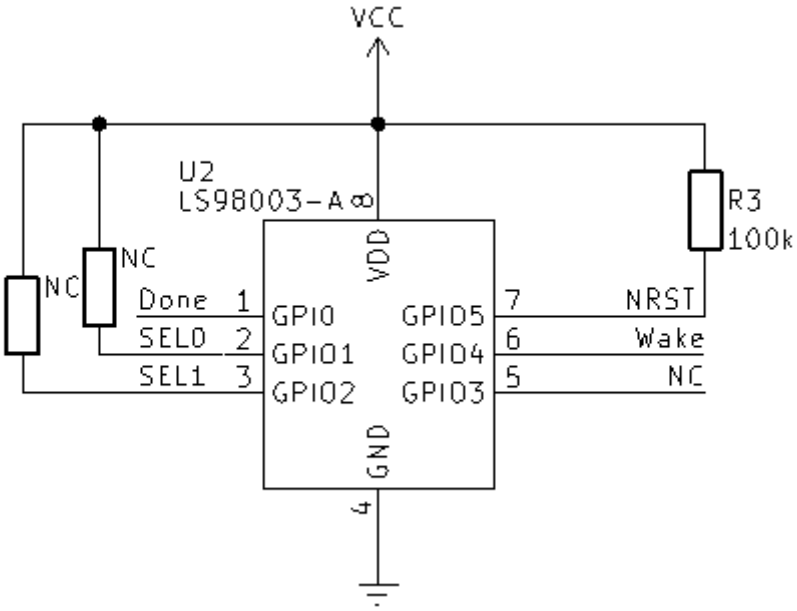
Program Code Version Information

Date	Datasheet Version	Programming Code Version	Lock Status	Checksum	Part Code	Code Version
2024-01-04	0.3	002	L	0XD7408FB	B28	B

Datasheet Revision History

Date	Version	Change
2022-12-22	0.1	Initial version, new design for LS98003-A chip
2023-09-03	0.2	Add test data
2024-01-04	0.3	Add LS98003-D package

LSS5010T-A
Reference Schematic



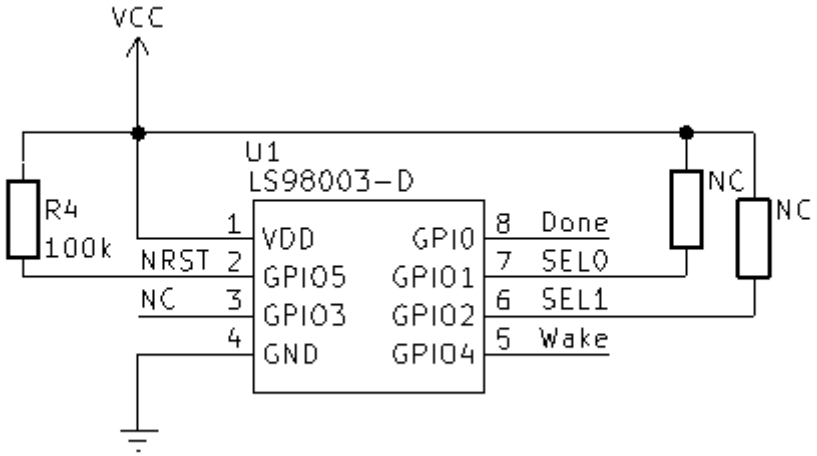
Note:

1. Voltage on any pin must be with in GND to VDD.
2. ESD protect is must be considered on all Pins which connected to external interface.

Pin name

Pin	Pin name	TYPE	Function
1	Done	2x Push Pull Digital Output	Digital signal driven by the µC to indicate successful processing of the WAKE signal.
2	SEL0	Without Schmitt trigger Digital input	Internal Pull- down 1M.
3	SEL1	Without Schmitt trigger Digital input	Internal Pull- down 1M.
4	GND	Power	Ground
5	NC	NC	NC
6	Wake	2x Push Pull Digital Output	Digital pulsed signal to wake up the µC at the end of the programmed time interval.
7	NRST	2x Open drain digital Output	NRST output
8	VCC	Power	Power supply input，1.8V~5.5V

LSS5010T-D
Reference Schematic



Note:

3. Voltage on any pin must be with in GND to VDD.
4. ESD protect is must be considered on all Pins which connected to external interface.

Pin name

Pin	Pin name	TYPE	Function
1	VCC	Power	Power supply input，1.8V~5.5V
2	NRST	2x Open drain digital Output	NRST output
3	NC	NC	NC
4	GND	Power	Ground
5	Wake	2x Push Pull Digital Output	Digital pulsed signal to wake up the µC at the end of the programmed time interval.
6	SEL1	Without Schmitt trigger Digital input	Internal Pull- down 1M.
7	SEL0	Without Schmitt trigger Digital input	Internal Pull- down 1M.
8	Done	2x Push Pull Digital Output	Digital signal driven by the µC to indicate successful processing of the WAKE signal.

Customize Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_Q	Quiescent Current	Static inputs and floating outputs, VDD=3.3V	--	3	--	μA
T_{wake}	SEL0=0, SEL1=0	At temperature 25℃	0.465	0.5	0.535	S
	SEL0=1, SEL1=0	At temperature 25℃	1.86	2	2.14	S
	SEL0=0/1, SEL1=1	At temperature 25℃	14.88	16	17.12	S
T_{nRST}	Low Reset Time	At temperature 25℃	297	320	329	mS

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
Supply Voltage on VDD to GND	-0.3	7	V
Maximum Voltage Input to Pins	--	VDD + 0.3	V
VDD to GND Maximum DC Current	--	90	mA
Input Leakage Current	--	1000	nA
Storage Temperature Range	-65	150	℃
Junction Temperature	--	150	℃
ESD Protection (HBM)	2000	--	V
ESD Protection (CDM)	500	--	V
Moisture Sensitivity Level (MSL)	1		

Electrical Characteristics

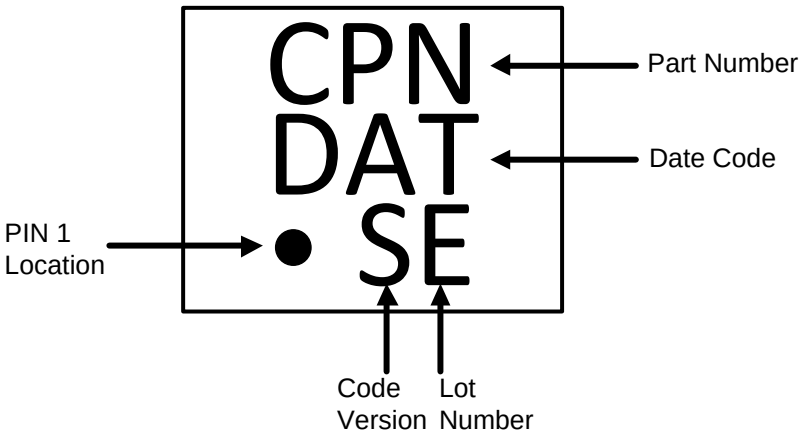
EC at T = -40℃ to +85℃, VDD = 1.8V to 5.5V Unless Otherwise Noted

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.8	5.0	5.5	V
T_A	Operating Temperature		-40	25	85	℃
C_{VDD}	Capacitor Value at VDD		--	0.1	--	μF
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_{VDD}	Maximum Average or DC Current Through VDD Pin	T_J = 85°C	--	--	90	mA
I_{IH}	HIGH-Level Input Current	Logic Input PINs; V_{IN} = VDD	-1.0	--	1.0	μA
I_{IL}	LOW-Level Input Current	Logic Input PINs; V_{IN} = 0V	-1.0	--	1.0	μA
V_{IH}	HIGH-Level Input Voltage	Logic Input without Schmitt Trigger, at VDD=1.8V	1.03	--	--	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
		Logic Input without Schmitt Trigger, at VDD=3.3V	1.85	--	--	V
		Logic Input without Schmitt Trigger, at VDD=5.0V	2.87	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input without Schmitt Trigger, at VDD=1.8V	--	--	0.72	V
		Logic Input without Schmitt Trigger, at VDD=3.3V	--	--	1.27	V
		Logic Input without Schmitt Trigger, at VDD=5.0V	--	--	1.98	V
V_{OH}	HIGH-Level Output Voltage	Push Pull, 2x Drive I_{OH} = 100uA, at VDD=1.8 V	1.70	--	--	V
		Push Pull, 2x Drive I_{OH} = 3mA, at VDD=3.3 V	2.80	--	--	V
		Push Pull, 2x Drive I_{OH} = 5mA, at VDD=5.0 V	4.20	--	--	V
V_{OL}	LOW-Level Output Voltage	Push Pull, 2x Drive I_{OL} = 100uA, at VDD=1.8 V	--	--	0.006	V
		Push Pull, 2x Drive I_{OL} = 3mA, at VDD=3.3 V	--	--	0.22	V
		Push Pull, 2x Drive I_{OL} = 5mA, at VDD=5.0 V	--	--	0.21	V
		Open Drain, 2x Drive I_{OL} = 100uA, at VDD=1.8 V	--	--	0.002	V
		Open Drain, 2x Drive I_{OL} = 3mA, at VDD=3.3 V	--	--	0.089	V
		Open Drain, 2x Drive I_{OL} = 3mA, at VDD=5.0 V	--	--	0.114	V
I_{OH}	HIGH-Level Output Current	Push Pull, V_{OH} = VDD-0.2, 2X Driver, at VDD=1.8 V	1.6	--	--	mA
		Push Pull, V_{OH} = 2.4 V, 2X Driver, at VDD=3.3 V	10	--	--	mA
		Push Pull, V_{OH} = 2.4 V, 2X Driver, at VDD=5.0 V	38	--	--	mA
I_{OL}	LOW-Level Output Current	Push Pull, V_{OL} = 0.15 V, 2X Driver, at VDD=1.8 V	2.1	--	--	mA
		Push Pull, V_{OL} = 0.4 V, 2X Driver, at VDD=3.3 V	10	--	--	mA
		Push Pull, V_{OL} = 0.4 V, 2X Driver, at VDD=5.0 V	14	--	--	mA
		Open Drain, V_{OL} = 0.15V, 2X Driver, at VDD=1.8 V	6.3	--	--	mA

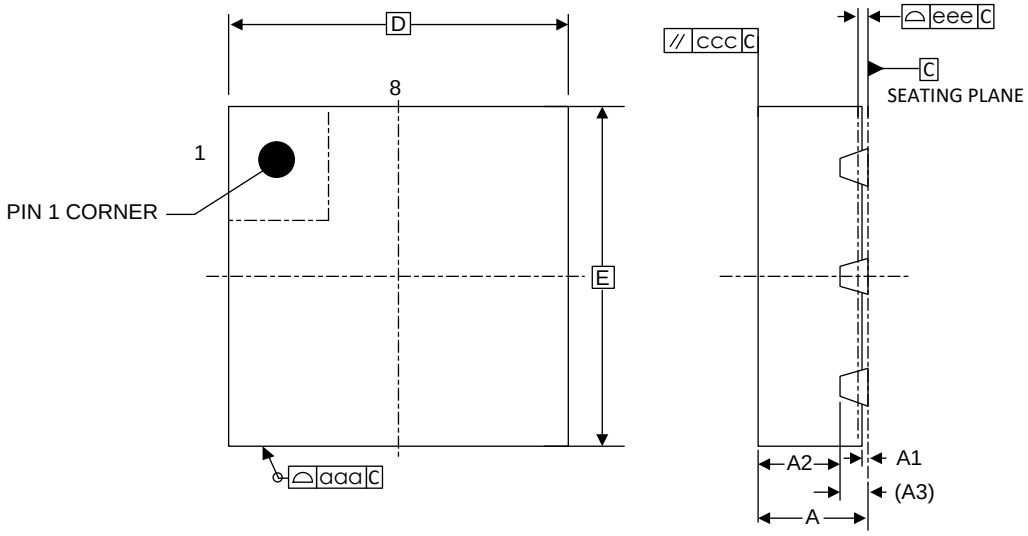
Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
		Open Drain, V_{OL} = 0.4 V, 2X Driver, at VDD=3.3 V	30	--	--	mA
		Open Drain, V_{OL} = 0.4 V, 2X Driver, at VDD=5.0 V	42	--	--	mA
R_{PULL}	Pull up or down Resistance	1Mohm Pull up or down	--	1	--	MΩ
		100Kohm Pull up or down	--	100	--	kΩ
		10Kohm Pull up or down	--	10	--	kΩ
T_{SU}	Startup Time	From VDD rising past PON threshold	--	1.20	--	mS
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.67	1.80	1.92	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.95	1.25	1.54	V
A_{HFOSC}	20KHz	VDD = 1.8V, T = 25℃	--	20.5	--	MHz
		VDD = 1.8V, T = -40℃~85℃	19.27	--	21.73	kHz
		VDD = 3.3V, T = 25℃	--	20	--	kHz
		VDD = 3.3V, T = -40℃~85℃	18.8	--	21.2	kHz
		VDD = 5.0V, T = 25℃	--	20	--	kHz
		VDD = 5.0V, T = -40℃~85℃	18.8	--	21.2	kHz

Package Top Marking

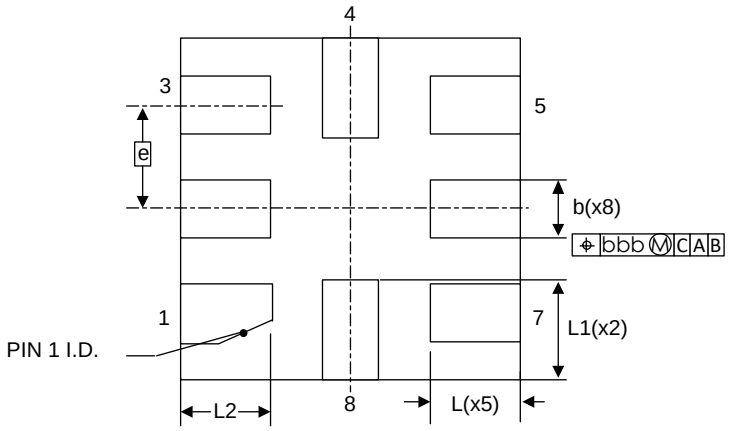


Package Drawing and Dimensions

TQFN-8L: 1.3×1.3×0.55mm, 0.4mm pitch(LS98003-A)



TOP VIEW SIDE VIEW

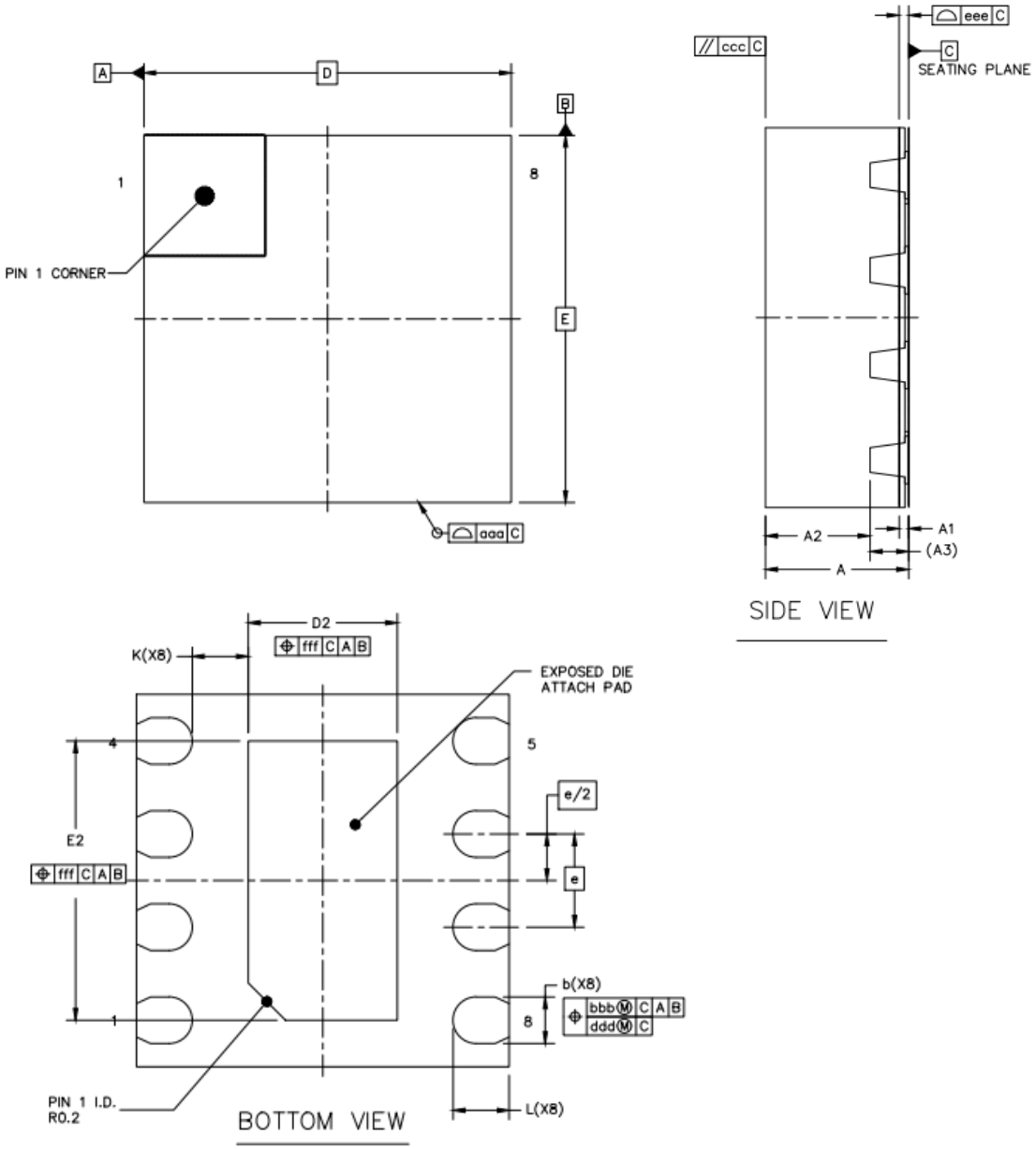


BOTTOM VIEW

Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.5	0.55	0.6	D	1.3BSC		
A1	0	0.02	0.05	E	1.3BSC		
A2	---	0.4	---	L	0.25	0.3	0.35
A3	0.152REF			L1	0.3	0.35	0.4
b	0.15	0.2	0.25	L2	0.2	0.3	0.4
aaa	0.1			bbb	0.1		
ccc	0.1			eee	0.05		
e	0.4 BSC						

DFN-8L: 2×2×0.75mm, 0.5mm pitch(LS98003-D)

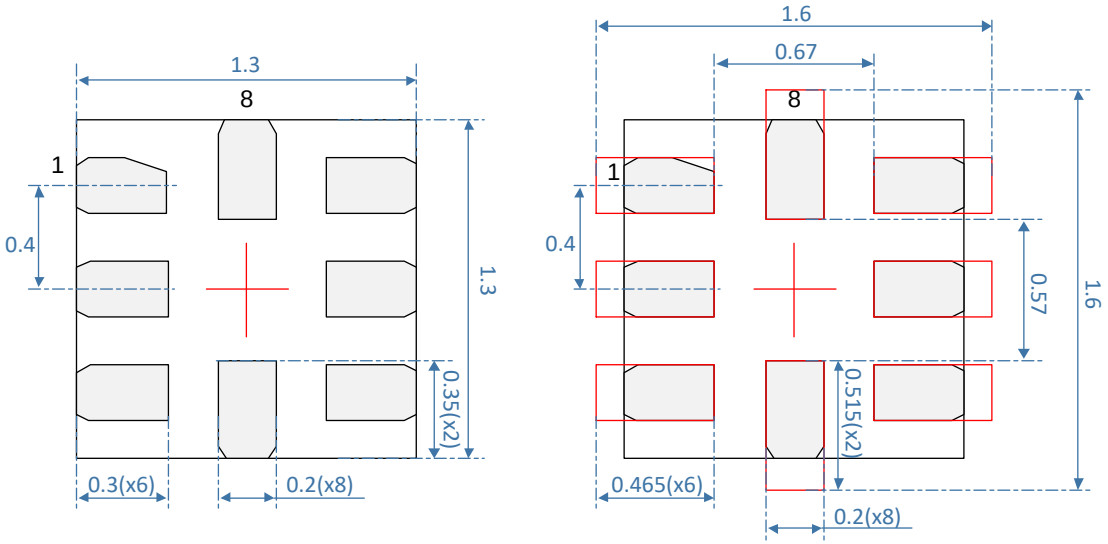


Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.7	0.75	0.8	D	2 BSC		
A1	0	0.02	0.05	E	2 BSC		
A2	---	0.55	---	L	0.2	0.3	0.4
A3	0.203 REF			D2	0.7	0.8	0.9
b	0.2	0.25	0.3	E2	1.4	1.5	1.6
aaa	0.1			bbb	0.1		
ccc	0.1			eee	0.05		
e	0.5 BSC						

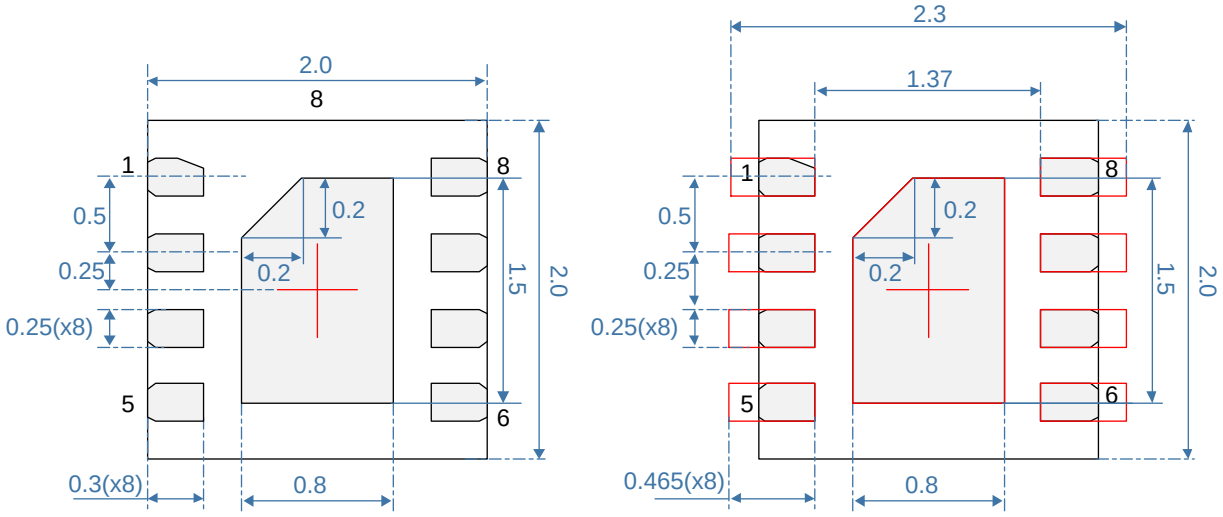
Recommended Land Pattern

LS98003-A



Unit: mm

LS98003-D



Unit: mm

Tape and Reel Information

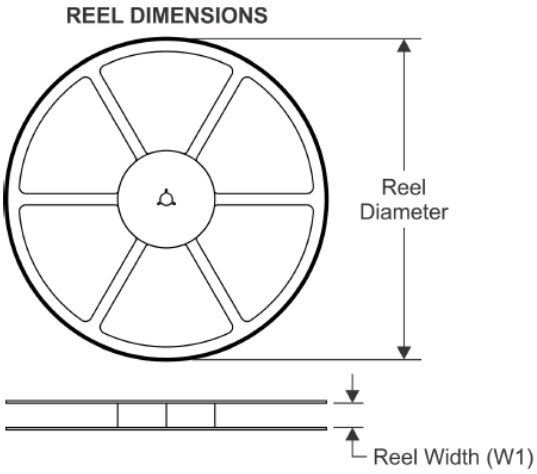
LS98003-A:

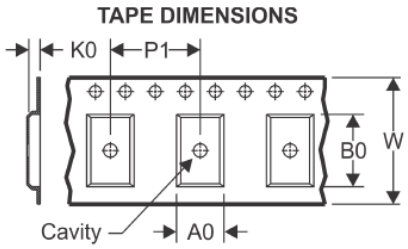
Package Type	Num of Pins	Package Size [mm]	Units/package		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			SPQ	1 Box		Pockets	Length [mm]	Pockets	Length [mm]		
TQFN-8L 1.3×1.3mm	8	1.3×1.3×0.55	3000	3000	178/60	30	120	140	560	8	4

LS98003-D:

Package Type	Num of Pins	Package Size [mm]	Units/package		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			SPQ	1 Box		Pockets	Length [mm]	Pockets	Length [mm]		
DFN-8L 2.0×2.0mm	8	2.0×2.0×0.75	3000	3000	178/60	30	120	140	560	8	4

Carrier Tape Drawing and Dimensions





LS98003-A:

A0	Dimension designed to accommodate the component width	1.6mm
B0	Dimension designed to accommodate the component length	1.6mm
K0	Dimension designed to accommodate the component thickness	0.8mm
W	Overall width of the carrier tape	8.0mm
W1	Reel Width	9.5mm
P0	Pitch between Index Hole Pitch	4.0mm
P1	Pitch between successive cavity centers	4.0mm

LS98003-D:

A0	Dimension designed to accommodate the component width	2.3mm
B0	Dimension designed to accommodate the component length	2.3mm
K0	Dimension designed to accommodate the component thickness	1.1mm
W	Overall width of the carrier tape	8.0mm
W1	Reel Width	9.5mm
P0	Pitch between Index Hole Pitch	4.0mm
P1	Pitch between successive cavity centers	4.0mm

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020